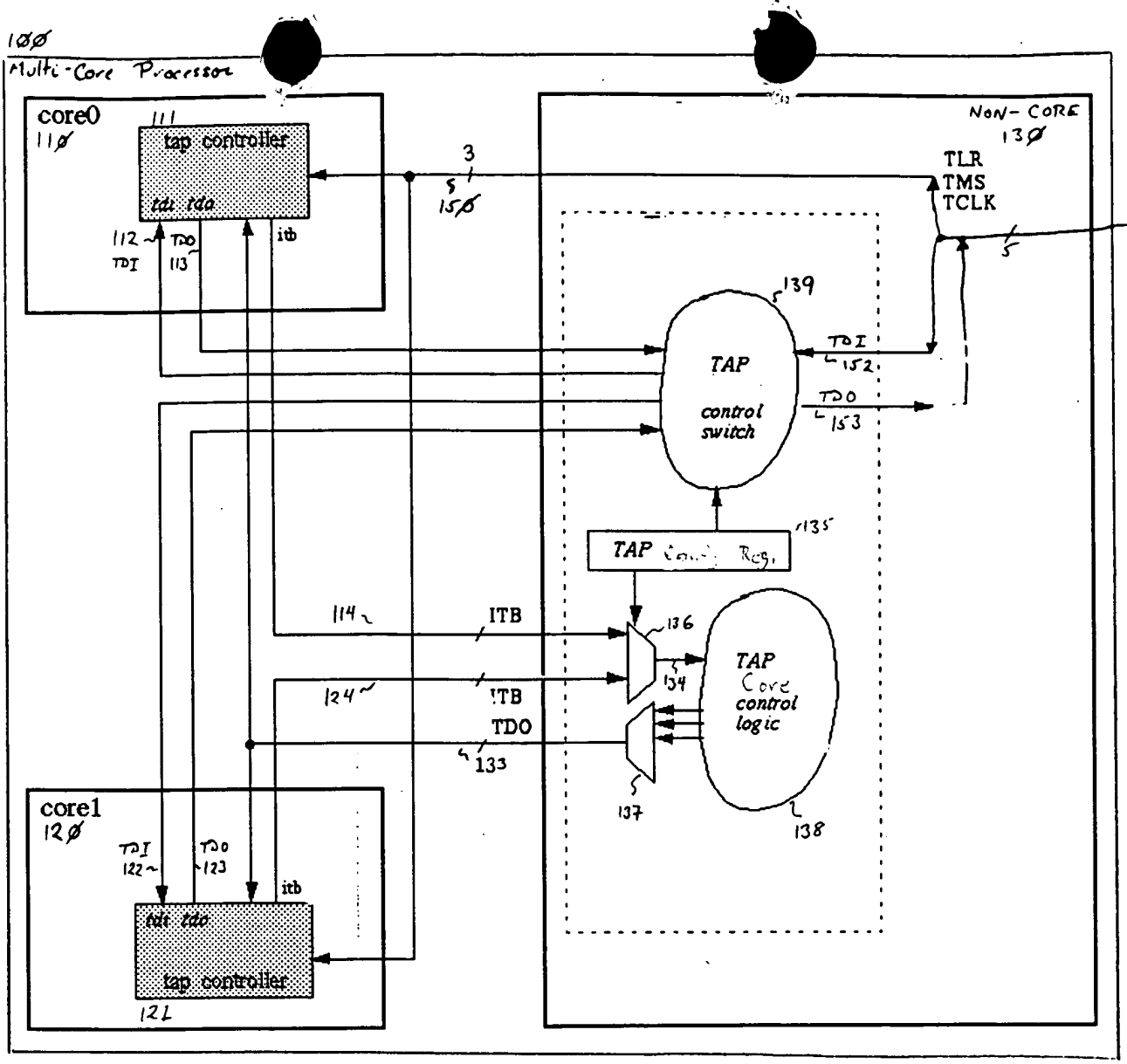

100
Multi-Core Processor
core0
110
111
tap controller
tdi tdo
112
TDI
TDO
113
itb
3
5
150
NON-CORE
130
TLR
TMS
TCLK
Pads
190
139
TAP
control
switch
TDI
152
TDO
153
135
TAP Control Reg.
114
ITB
136
134
124
!TB
TDO
133
TAP
Core
control
logic
137
138
core1
120
TDI
122
TDO
123
itb
tdi tdo
tap controller
121

FIG. 1

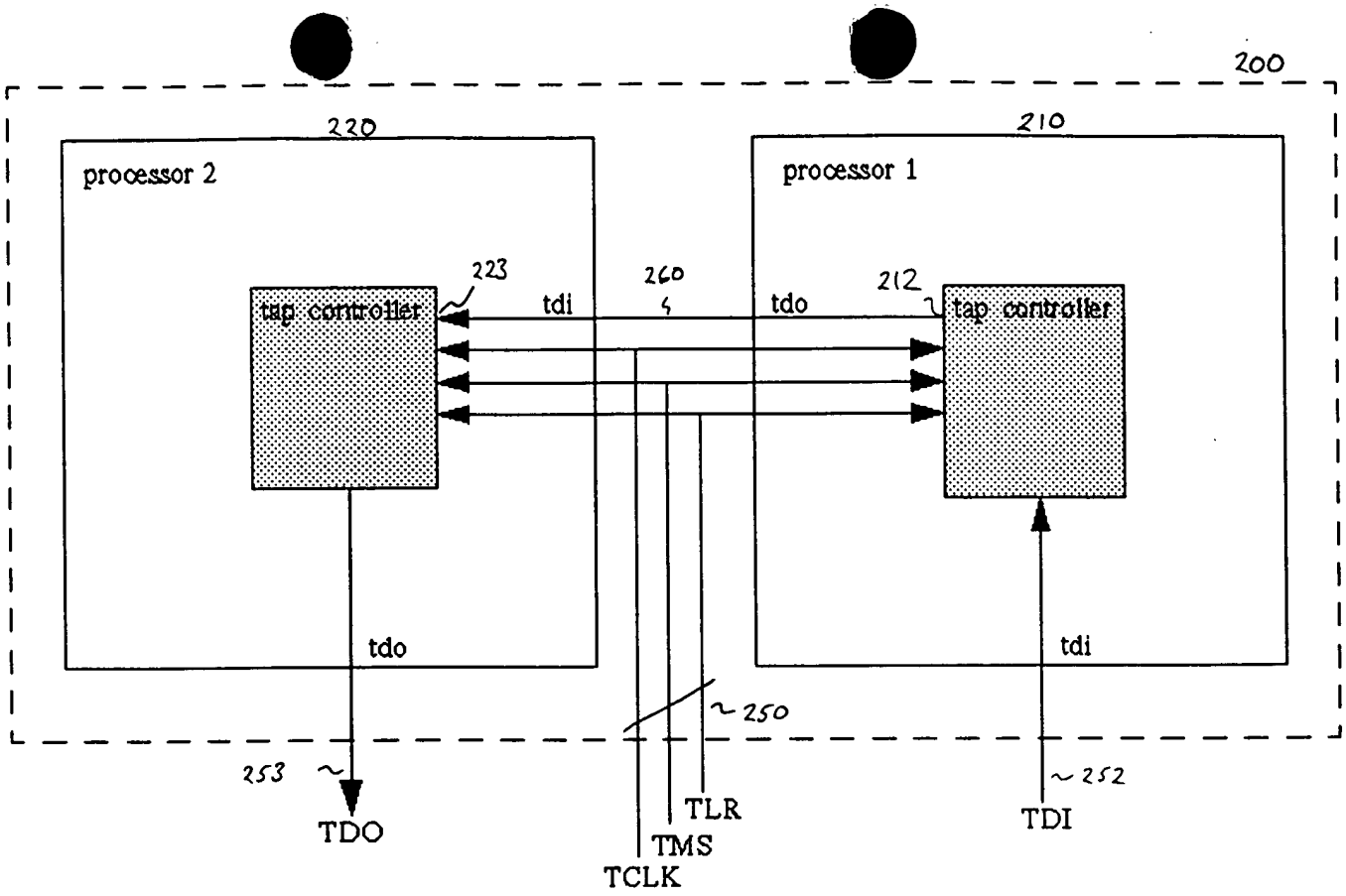

200
220
processor 2
210
processor 1
223
tap controller
tdi
260
tdo
212
tap controller
tdo
tdi
250
253
252
TDO
TLR
TMS
TCLK
TDI

FIG. 2

Fig 3a

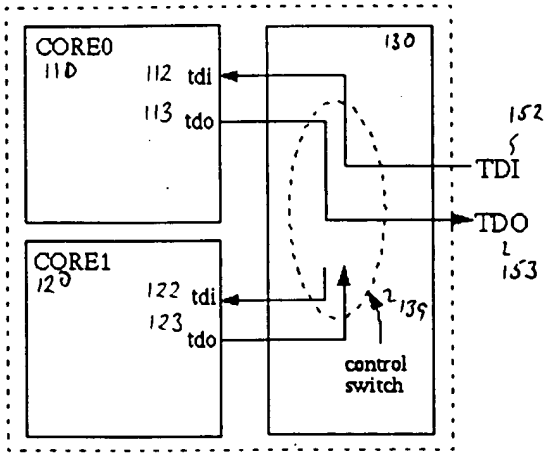
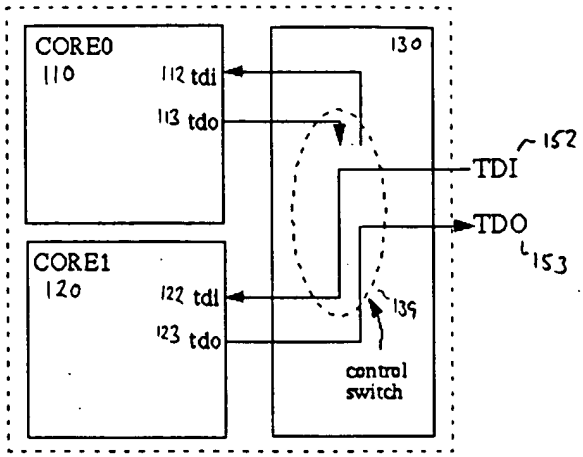


Fig 3b



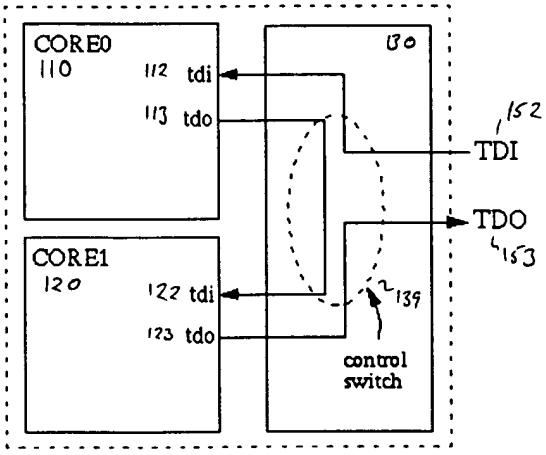


Fig 3c

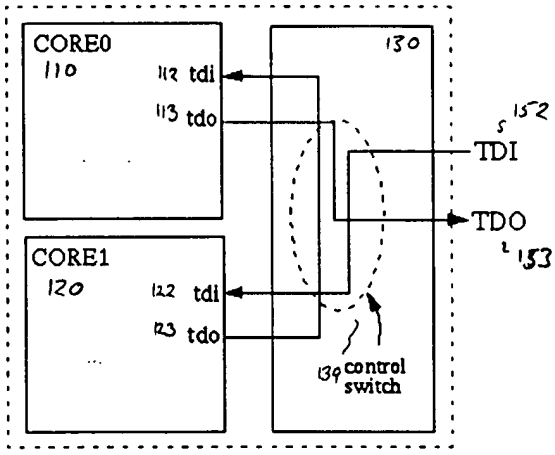


Fig 3d

Fig. 4a

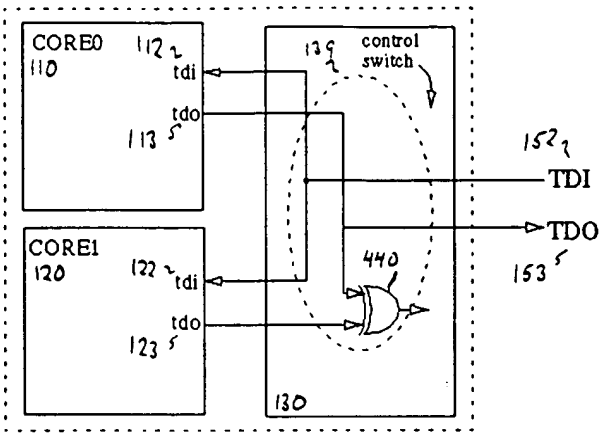
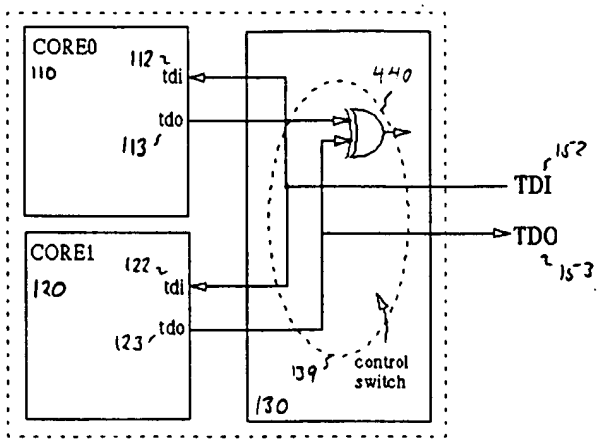


Fig 4b



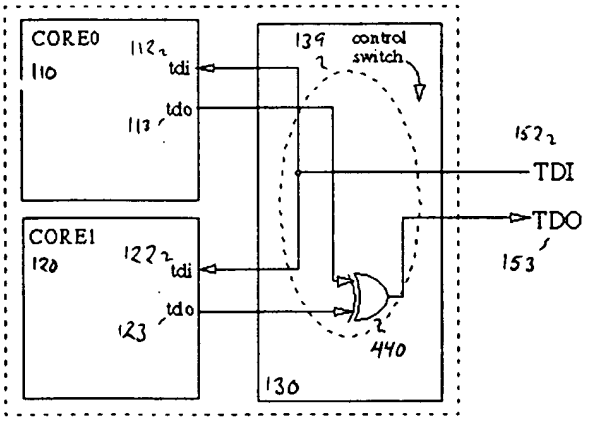


Fig 4c

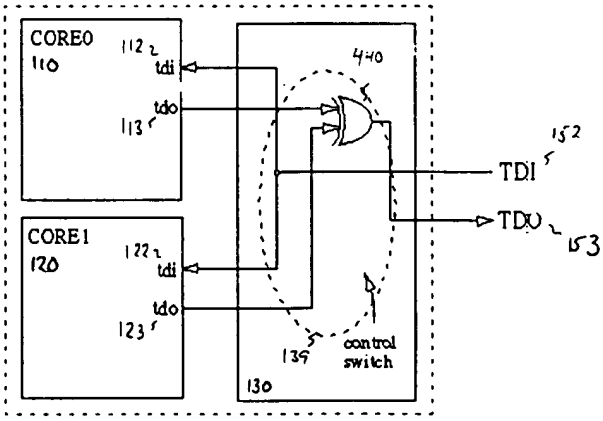


Fig 4d

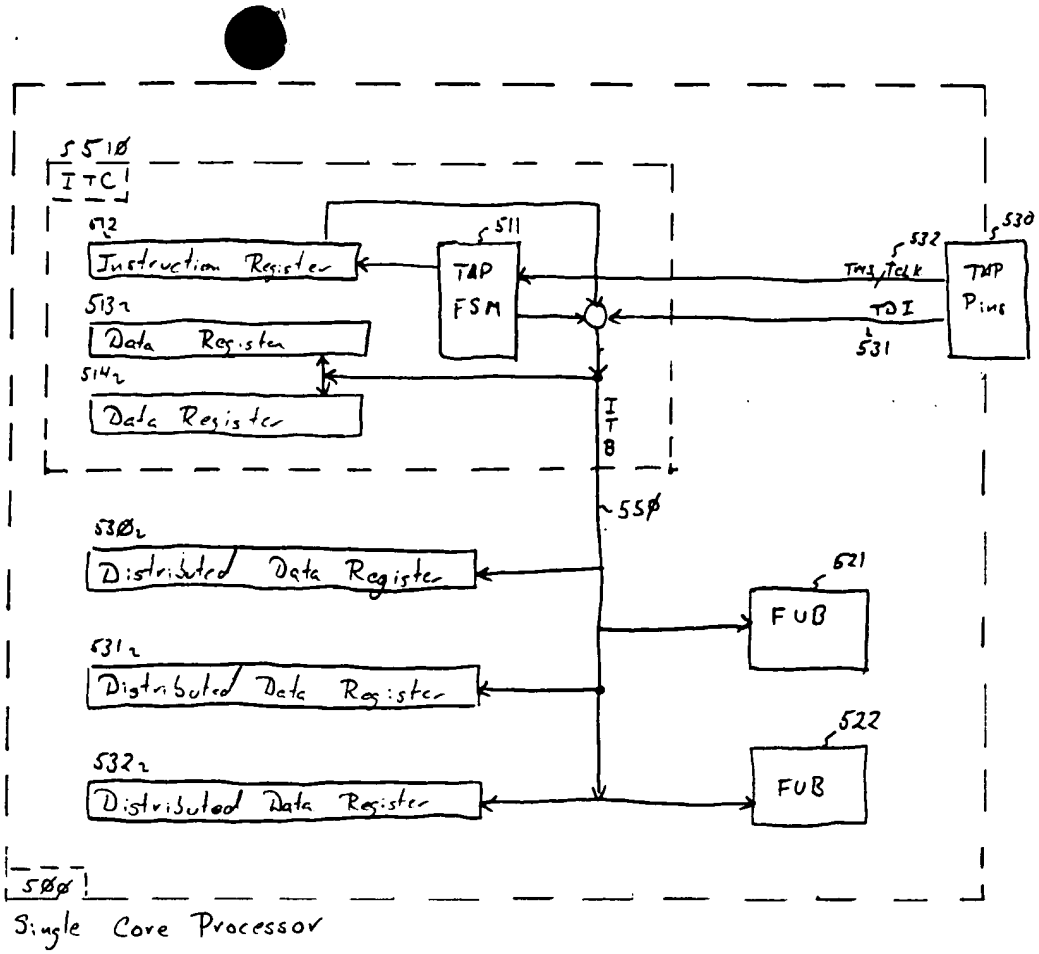
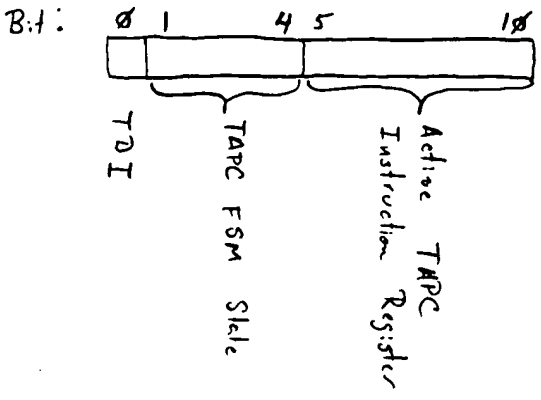

510
ITC
512
Instruction Register
511
TAP
FSM
530
532
TMS/TCLK
TAP
Pins
TDI
531
513
Data Register
514
Data Register
ITB
550
530
Distributed Data Register
621
FUB
531
Distributed Data Register
522
532
Distributed Data Register
FUB
500
Single Core Processor

Fig. 5

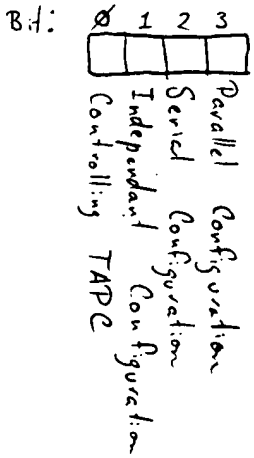
Fig. 6



Integrated Test Bus

Fig. 7

TAP Core Configuration Register



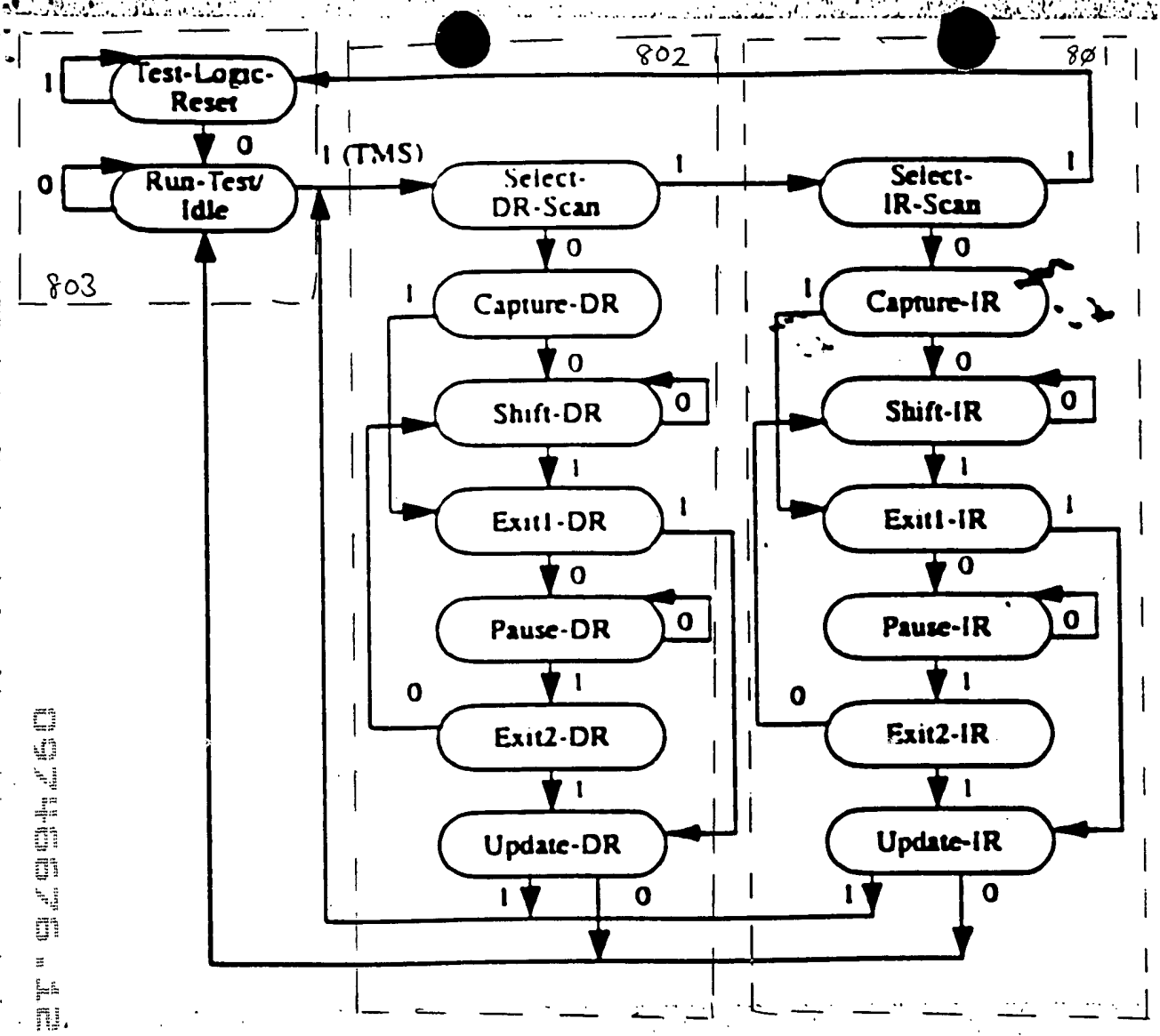

802
801
803
Test-Logic-Reset
Run-Test/ Idle
1 (TMS)
Select-DR-Scan
Capture-DR
Shift-DR
Exit1-DR
Pause-DR
Exit2-DR
Update-DR
Select-IR-Scan
Capture-IR
Shift-IR
Exit1-IR
Pause-IR
Exit2-IR
Update-IR

Fig. 8

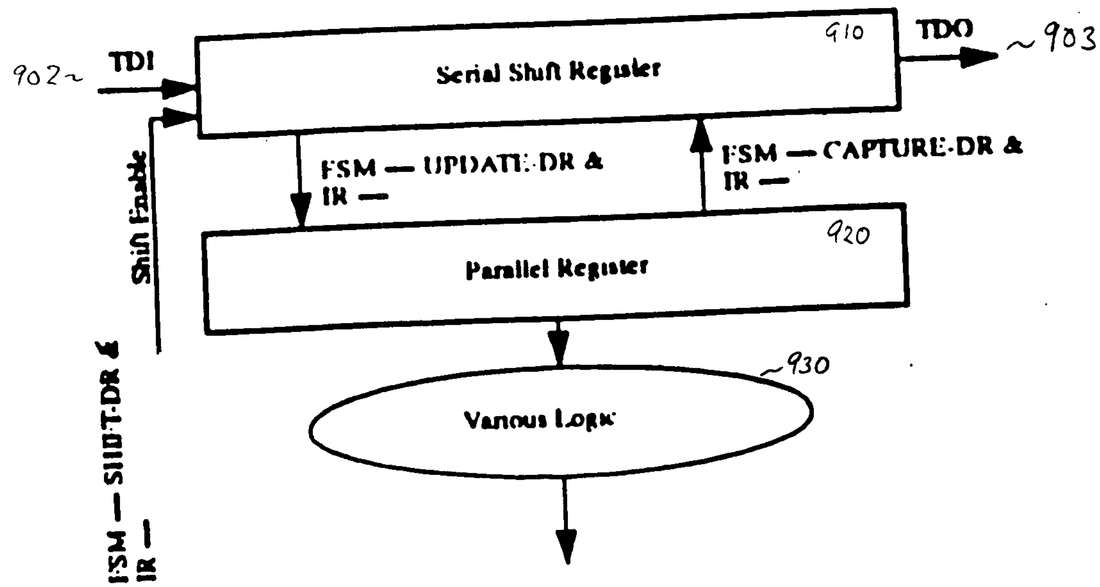

TDI
902
Serial Shift Register
910
TDO
903
FSM — UPDATE-DR &
IR —
FSM — CAPTURE-DR &
IR —
Shift Enable
FSM — SHIFT-DR &
IR —
Parallel Register
920
Various Logic
930

Fig. 9